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Soft Error-Aware Leakage Reduction through Body Bias

Warin Sootkaneung[1]*, Suppachai Howimanporn[2] and Sasithorn Chookaew[2]

[1] Faculty of Engineering, Rajamangala University of Technology Phra Nakhon
1381 Pracharat 1 Road, Wong Sawang, Bang Sue, Bangkok, Thailand 10800
[2] Faculty of Technical Education, King Mongkut's University of Technology North Bangkok
1518 Pracharat 1 Road, Wong Sawang, Bang Sue, Bangkok, Thailand 10800

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Abstract

For modern processors, two reliability issues, namely increased leakage power and soft error rate, continue to intensify as device technologies scale down to nanometers. While many researchers have proposed methods to efficiently control leakage power by tuning body bias, few recent works have considered the quantitative negative impact of this technique on circuit soft error vulnerability. In this paper, we introduce a novel body bias based approach for reliability improvement that correlates leakage reduction and soft error immunity degradation. The experimental results show that the proposed technique provides satisfactory leakage reduction with confined soft error degradation in 32 nm high-k/metal gate benchmark circuits.

Keywords: Soft Error; Leakage; Body Bias

**** Corresponding Author. Tel.: +668 3029 2275, E-mail Address**: warin.s@rmutp.ac.th*

1. Introduction

As device geometries of modern processors are decreasing into small nanometers to achieve system integration and performance requirements, the device threshold voltage (V_{th}) is scaled down to maintain an appropriate gate overdrive [1]. This leads to an exponential increase in leakage power which becomes the largest portion of overall chip power consumption. Elevated leakage power causes significant decrease in battery life for portable devices [2]. It can also break connections at gate terminals, inducing partial and full open defects for a wide spectrum of technologies [3]. To stabilize circuit thermal reliability due to leakage power, the additional cost of cooling and packaging design is also required. Leakage power dissipation considerably influences the permanent failure rate of a circuit. As a result from leakage power, the elevation in temperature is a main factor of most permanent failure mechanisms including electromigration, negative bias temperature instability, thermal cycling, and time-dependent dielectric breakdown.

One of the most successful leakage reduction approaches in circuit design phase employs body bias (BB) tuning based techniques since they require low area overhead [4] while returning high gain. Various BB based leakage reduction techniques, performing in both design time and run time environments, have recently been proposed [4] - [10]. These works selectively adjust device V_{th} by varying device BB which, in turn, alters the leakage and performance profile of the device. Specially, when reverse BB (RBB) is applied to a device, V_{th} increases. The increase in V_{th} causes the leakage to reduce but the delay to increase. On the other hand, forward BB (FBB) lowers device V_{th} and hence, timing performance is enhanced at the expense of an increase in leakage.

In addition to leakage problem, soft errors causing transient failures are considered as one of the equally or even more important reliability issues. How to moderate neutron-induced soft errors is becoming increasingly crucial and challenging due to the fact that modern circuits are more vulnerable to soft errors as device geometry is shrinking. Furthermore, most circuit parameter tuning approaches which require changes in bias condition, e.g. body bias, to enhance either reliability or performance may immensely affect the circuit soft error rate (SER). Primarily, circuit SER due to particle strike is relatively high compared to hard error rate due to increased power and temperature [11], [12]. As a result, soft error issue today adds more complexity to the design for reliability, and turns into a major burden for circuit designers to surpass. Unfortunately, few works related to leakage and SER reduction have associated the impact of one on each other.

The interdependence of BB and SER is well known [1], [13] - [15], yet the quantitative relation between the two was lately introduced by Fuketa et al. [14]. Focus of [14] is mainly to show that SER of SRAM cells increases significantly as the supply voltage decreases. However,

they continued to reveal that when the SRAM operates at normal supply voltage, BB also substantially influences SER. In the work published in [15], a method of minimizing leakage current through RBB subject to a bound on the SER for combinational circuits was proposed.

Unlike [15], in this study, our work introduces a heuristic based leakage reduction which involves the effect of soft error by selectively providing either FBB or RBB to each part of a combinational circuit fabricated with 32 nm high-k/metal gate technology. This proposed approach can reduce the leakage power more efficiently because it can search for the proper solution with the larger margin of BB variation.

The rest of this paper is organized as follows. Section 1.1 provides the motivations leading to this study. Section 1.2 shows leakage and soft error models and related theories. Sections 2 discusses the proposed approach for leakage reduction through body bias with soft error interrelation. Next, the experimental results and discussions are reported in sections 3. We finally conclude the study in section 4.

1.1 Motivations

From device level simulation in [15], it was found that the BB can alter the circuit SER. In particular, the critical charge (Q_{crit}) of a gate decreases when stronger RBB is applied, which subsequently causes SER to increase. When we expanded investigation domain from RBB to FBB region, we also found that stronger FBB reduces soft error glitch

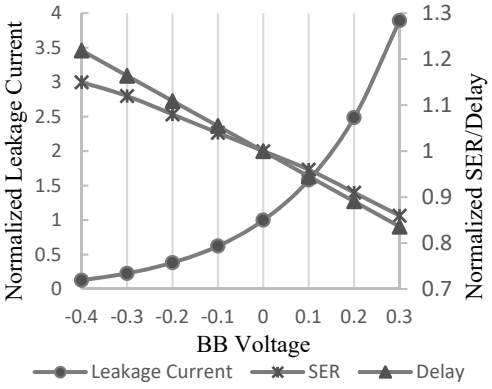

Fig. 1 Normalized leakage current, SER, and delay vs. BB voltage plots for the circuit c17

generation. The evidence of the above statement is shown in Fig. 1. This figure plots the normalized leakage current, SER, and delay as a function of BB for the circuit c17 mapped with 32-nm high-k/metal gate technology from [16]. It can be seen from Fig. 1 that when BB voltage of all gates in the circuit is in RBB region (Negative Values), leakage current decreases whereas SER and delay increase. On the other hand, in FBB region (Positive Values), the circuit c17 has a sharp increase in leakage current but its SER and delay decrease constantly.

This motivated us to study the joint effect of these two on circuit reliability improvement. The goal of this study is to find a leakage reduction method that compromises the opposite outcomes of BB on leakage and SER with acceptable or zero performance overhead. Moreover, it must be efficient on its scalability and CPU runtime, and hence, it can be applied to large circuits.

1.2 Related Theories

This section briefly discusses leakage and soft error models used in this study.

A. Leakage Model

The leakage current of a gate i, $I_{leak,i}$ can be expressed as a function of BB voltage of this gate, $V_{BB,i}$. During SPICE simulation, we separately test all the gates in the library with the input such that each gate has the worst case leakage. The relationship between $I_{leak,i}$ and $V_{BB,i}$ is then fitted into an exponential equation as shown in (1).

$$I_{leak,i} = \alpha + \beta e^{\gamma V_{BB,i}} \quad (1)$$

In (1) α, β, and γ are positive constants. For FBB, $V_{BB,i}$ has a positive value whereas for RBB, $V_{BB,i}$ is negative. From (1), we can further obtain the total leakage current in a silicon cell in the circuit by summing $I_{leak,i}$ for all gates. Since the leakage power of each gate i is the product of $I_{leak,i}$ and supply voltage, $V_{DD,i}$, the leakage power consumed by a cell, $P_{leak,cell}$ can be achieved by summing the leakage power of each gate as given in (2).

$$P_{(leak,cell)} = \sum_{i=1}^{total\ \#\ of\ gates} (I_{leak,i} * V_{DD,i}) \quad (2)$$

An increase in leakage power raises the temperature of a circuit block [17]. Subsequently, elevated temperature deteriorates long term reliability of the circuit. The relation of the changes in temperature and leakage power can be explained using a large thermal cycle model for mean time to failure (MTTF) in [18].

B. Soft Error Model

A particles strike, around reverse-biased p-n junction of a victim device, triggers a nuclear reaction and generates the amount of charge deposition at the junction [19]. This charge consequently induces a transient glitch at the drain of the device. For alpha particles, the generated glitch can be modeled as a double-exponential current injecting into the transistor drain [20]. For the case of neutron strike as focused in this study, a single-exponential current model as given in (3) is used [15], [21], [22].

$$I(t) = \frac{Q}{\tau}\sqrt{\frac{t}{\tau}}e^{-\frac{t}{\tau}} \quad (3)$$

In (3), Q is the amount of charge deposition and τ is the technology dependent charge-collection time constant. If the amount of charge deposition Q is sufficiently large, it can cause a transient flip in the output voltage of a gate. Since we assume that a gate fails when the output voltage changes to $V_{DD}/2$, we define the Q_{crit} as the amount of Q that can bring the output voltage to this level. For each gate type, in additional to the dependency of Q_{crit} of a node (a transistor) on the BB, the Q_{crit} also depends on gate input [12], [23], [24].

An energy transfer model from [19] is adopted to obtain the energy of the striking particle which produces Q_{crit} or causes a circuit to fail. The terrestrial

neutron flux above the minimum energy that can upset the circuit (corresponding to the Q_{crit} as discussed above) can be collected using the JEDEC89A standard [25]. Since the neutron flux represents a strike rate per unit area, calculation for the rate of single event transient (SET) generation requires the *active area*, the area where the strike occurs. The actual active area is the region near reverse-biased junction of each CMOS transistor but we simply use the transistor drain area as an approximation. The equation given below provides the SER of a node *k* in a gate *i* when an input vector *j* is applied [12], [24].

$$NodeSER_{i(j,k)} = R_{(Qcrit)_{i(j,k)}} * P_{SE_{i(j,k)}} \quad (4)$$

$R_{(Qcrit)_{i(j,k)}}$ is the rate of SET generated from a strike at a node *k* in a gate *i* as expressed in (5). $P_{SE_{i(j,k)}}$ is the soft error probability which includes electrical, logical, and timing window masking probabilities of a circuit [26].

$$R_{(Q_{crit})_{i(j,k)}} = \left(\int_{Q_{crit}}^{\infty} \frac{d\phi_{i(j,k)}(q)}{dq} dq \right) * Ad_{i(k)} \quad (5)$$

In (5), the integrand of integral term is the differential terrestrial neutron flux, $\frac{d\phi_{i(j,k)}(q)}{dq}$, which can be obtained from [19], [25]. The result of the integration is the total neutron flux, having energy above the energy of Q_{crit}, indicating the rate of strike per unit area. $Ad_{i(k)}$ is the area of node *k* (the drain area of the victim transistor) in gate *i*.

We define the SER of a gate *i*, $GateSER_i$ as the summation of SER at each node *k* in the gate *i* in (4) as given in (6)

$$GateSER_i = \sum_{i(j)} \sum_{i(k)} NodeSER_{i(j,k)} \quad (6)$$

The SER of a circuit, *Circuit SER*, can be expressed as the summation of SER of each gate *i* in (6) as shown in (7) below.

$$Circuit\ SER = \sum_i Gate\ SER_i \quad (7)$$

2. Research Methodology

Our proposed technique primarily focuses on decreasing the amount of leakage current while limiting the increase in SER of each gate, and strictly maintaining critical delay of the original circuit. This method is developed on the basis that large RBB should be assigned to gates that have sharp leakage reduction gain, but are less sensitive to soft error. Hence, we can reduce large amount of leakage current of these gates without significantly impacting the SER. On the other hand, some gates that have small leakage reduction gain but high soft error sensitivity are assigned large FBB. For this reason, they are good candidates for recovering the circuit delay without high cost of increased leakage.

Fig. 2 shows the flowchart of our proposed soft error-aware leakage reduction method. First, the original critical delay of a circuit and SER of each gate with zero body bias (ZBB) condition

are computed. Next, all gates which are most sensitive to soft error (the number of these gates is defined by the user) are initially assigned the largest FBB level. The purpose of this step is to lower soft error rate of the circuit by treating only few vulnerable gates. The other gates, which are less sensitive to soft error, are then assigned the largest RBB to gain leakage reduction. Since gate and circuit delay increases as device BB is moving towards RBB, the following steps are required to recover the excessive delay and maintain the overall timing performance.

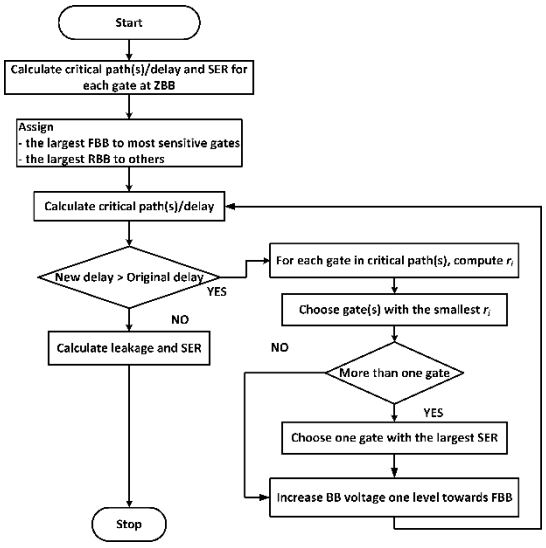

Fig. 2 Flowchart of the proposed soft error-aware leakage reduction

In the delay recover process, we start the first iteration by extracting new critical delay of the circuit. The new critical delay is then checked whether, as a result of assigned RBB, it is larger than the original critical delay or not. If the new critical delay is lower or equal to the original critical delay, the algorithm is complete. However, if the new critical delay is greater than the original delay, BB of some gates must be increased towards FBB to recover the circuit performance. The procedure for selecting the gates to improve the delay is as follows. In each round of iterations, we search for a gate in the new critical path(s) that has the smallest leakage increasing rate, r_i, with respect to its FBB. The value of r_i can be obtained by finding the derivative of $I_{leak,i}$ in (1) with respect to $V_{BB,i}$ as given in (8).

$$r_i = \left.\frac{\partial I_{leak,i}}{\partial V_{BB,i}}\right|_{V_{BB,i}=assigned\ \mathrm{BB}} \tag{8}$$

If more than one gate has the same r_i, the gate with the highest soft error sensitivity or the largest SER is selected. Once such a gate is found, we increase its BB one step towards FBB to make this gate faster. We iteratively search for new critical path(s), update gate delay, and readjust the BB of the candidate gate until the delay performance is satisfied.

3. Results and Discussions

After extensive device level simulation to obtain the relationship between BB and leakage as well as Q_{crit} information, the gate level framework was implemented with JAVA codes in a 4-GHz, Intel Quad-Core machine with 12-GB SDRAM. The cell library used in each experimental circuit consists of 2-input, 3-input, and 4-input NAND and NOR gates, and Inverters. Those cells are mapped

with 32-nm high-k/metal gate technology from [16]. The experimental circuits are selected from the ISCAS-85/89 (combinational parts) and MCNC benchmark suits. All reported results are also normalized with respect to baseline configuration in which all devices have ZBB. In this section, we first provide the results of leakage reduction from our proposed technique applied to selected benchmark circuits. Next, effect of available BB voltage levels on reliability gain is investigated. Finally, we discuss some important remarks.

3.1 Experimental Results

Table 1 shows the normalized results of delay, leakage current, and SER and CPU time from our proposed approach, which takes the impact of soft error into consideration. These results are compared to those from the method in which soft error degradation due to the change in BB is not involved. In this experiment, we allow BB to be available in the steps of 0.1 V within the range of minimum and maximum BB of -0.4 and 0.3 V, respectively. The BB of top 1-10% of the most sensitive gates is initially assigned with 0.3 V which is the maximum FBB considered in this study. Also, both methods strictly keep delay performance unchanged. It is evident from Table 1 that our proposed method can reduce the leakage up to 70% while SER is maintained or even decreased in some circuits. On the other hand, the other method yields larger leakage reduction, yet SER of all of the experimental circuits increases by 7% to 9%.

Table 1. Results of normalized delay, leakage, and SER, and CPU time for selected benchmark circuits

Circuit	Soft error-aware leakage reduction				Leakage reduction without soft error consideration			
	Delay	***Leakage***	***SER***	***CPU time (s)***	***Delay***	***Leakage***	***SER***	***CPU time (s)***
C499	1.00	0.61	0.99	10.97	1.00	0.56	1.07	11.46
C880	1.00	0.68	1.00	2.26	1.00	0.23	1.09	2.29
C1355	1.00	0.77	0.99	12.94	1.00	0.75	1.08	13.90
C1908	1.00	0.35	1.00	3.35	1.00	0.25	1.08	3.54
C5315	1.00	0.30	0.99	50.90	1.00	0.18	1.09	52.64
C6288	1.00	0.66	1.00	182.91	1.00	0.39	1.08	200.70
S208	1.00	0.53	1.00	0.17	0.99	0.24	1.08	0.19
S838	1.00	0.48	0.99	1.46	1.00	0.21	1.09	1.43
S13207	1.00	0.50	0.99	169.60	1.00	0.14	1.09	186.67
S15850	1.00	0.52	1.00	433.00	1.00	0.15	1.09	463.22
i1	1.00	0.67	0.98	0.08	1.00	0.29	1.09	0.08
i2	1.00	0.52	0.97	1.28	1.00	0.62	1.09	1.51
i3	1.00	0.70	0.97	0.53	1.00	0.62	1.08	0.61
i4	1.00	0.45	0.99	1.07	1.00	0.35	1.08	1.20
i5	0.99	0.91	1.00	0.31	1.00	0.15	1.09	0.32
i6	1.00	0.54	1.00	10.16	1.00	0.41	1.08	10.74
i7	0.98	0.56	1.00	12.08	1.00	0.38	1.08	13.90
i8	1.00	0.37	0.98	72.20	1.00	0.24	1.08	75.87

We further investigate the impact of available BB levels on leakage reduction. Fig. 3 plots the decrease in leakage current of the circuit i2. In this experiment, a number of BB configurations, containing different sets of available BB voltages, shown below the horizontal axes of the bar charts in Fig. 3, are assigned to the circuit. It can be seen from Fig. 3 that choices of BB voltage levels have little impact on the results. The leakage reduction gain drops from 48% to 42% for some BB configurations. The advantage for having the small number of available BB voltage levels is that the overall layout cost and routing and placement complexities are reduced substantially. We believe that our proposed technique will retain this benefit without significant impact on leakage improvement yield.

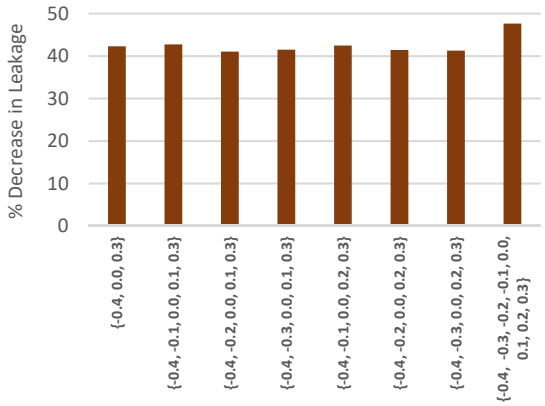

Fig. 3 Percentage decrease in leakage current of the circuit i2 for different sets of BB voltages

Table 2 contains the normalized results of delay, SER, and leakage current, and CPU runtime for all experimental circuits using the proposed approach with reduced number of available BB voltage levels. In this investigation, we allow BB voltages of {-0.4, 0.0, 0.3} V. to be available for each gate. Compared with the results in Table 1 which requires more BB voltage levels (all increments of 0.1 V. between -0.4 and 0.3 V.), in most cases, the leakage reduction results in Table 2 are close to those from the previous experiments. Additionally, the CPU time required for solving the problem for each circuit decreases substantially, since fewer voltage levels reduce the number of iterations during delay recovery process.

Table 2. Leakage reduction with three available BB voltages

Circuit	Delay	Leakage	SER	CPU Time (s)
C499	1.00	0.75	0.99	3.17
C880	1.00	0.73	1.00	0.75
C1355	1.00	0.86	0.99	3.60
C1908	1.00	0.38	1.00	0.94
C5315	1.00	0.31	0.99	15.30
C6288	1.00	0.76	1.00	49.77
S208	1.00	0.56	1.00	0.08
S838	1.00	0.52	0.99	0.56
S13207	1.00	0.50	0.99	45.42
S15850	1.00	0.53	1.00	139.77
i1	1.00	0.72	0.98	0.05
i2	1.00	0.58	0.97	0.39
i3	1.00	0.69	0.97	0.21
i4	1.00	0.47	1.00	0.37
i5	1.00	0.91	1.00	0.17
i6	1.00	1.00	1.00	4.44
i7	1.00	0.65	1.00	3.50
i8	1.00	0.50	0.98	26.09

3.2 Discussions

In the proposed technique, we initially assigned the maximum FBB

voltage to 1-10% gates with highest soft error vulnerability for all experimental circuits. Although the best number of those candidate gates varies from circuit to circuit and is difficult to determine, this setting can provide satisfactory leakage reduction gain under SER and delay constraints.

The importance of addressing leakage and soft error together arises from the fact that BB based techniques can improve one of these two problems while worsening the other. For example, from Table 1, applying leakage reduction approach without SER consideration on the circuit c1908 yields as much as 75% leakage reduction, yet the SER increases by 8%. On the other hand, without SER consideration, our proposed method maintains the SER, but lowers the leakage by only 65%. Although we can achieve large improvement when we solely manage leakage without soft error concern, the side effect of increased soft error vulnerability on the circuit cannot be neglected. The impact of soft error on overall circuit reliability in term of MTTF is relatively high compared to leakage problem [15]. However, it is quite difficult to directly determine the comparative priority of both issues as a result of the variety of systems and their applications. For instance, transient soft error may be uncontrollable and possibly severe for some life-critical systems such as aviation systems and medical instruments, whereas leakage problems influence battery consumption for mobile devices and long term permanent failure due to increased temperature. This proposed technique, one of the early works that take into consideration both leakage and soft error, can pleasantly resolve this issue.

BB based leakage reduction may increase the cost of implementation of the separated body parts and power supply which is not taken into account in this work. However, due to its impressive outcomes for leakage control, this work provides insightful start to the future direction of integrated reliability management.

4. Conclusion

This paper investigates the effects of leakage and soft error on circuit reliability and proposes a technique for limiting leakage current by adjusting the BB. In our method, we make use of the observation that larger RBB assigned to a gate reduces the leakage but causes SER to increase, whereas larger FBB causes the opposite consequence. In order to combine the above impacts, we develop a novel BB based approach for leakage reduction which involves soft error sensitivity degradation during BB adjustment in digital circuits. The proposed technique can efficiently arrange the BB voltage of each gate to moderate leakage current while strictly conserving the circuit SER and performance. The experimental results show that the proposed technique accomplishes a large decrease in leakage current and is scalable for large circuits due to its CPU runtime efficacy. Further,

the impact of the number of available BB voltage level is investigated and found that leakage reduction gain from our technique applied to the circuit with reduced BB voltage levels drops slightly compared to the gain of the circuit with large number of available BB voltage levels. Hence, this technique also helps reduce routing and placement cost while resulting satisfactory leakage reduction outcome.

5. Acknowledgment

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